Application No.: 09/438,295 Docket No.: 21737-00013-US

AMENDMENTS TO THE CLAIMS

Claims 1-5 cancelled

6. (Currently amended)A computer readable medium storing program code for causing a computer to write data of bits in a semiconductor device having a plurality of multilevel memory cells, each cell storing at least three levels of data each, comprising:

first program code means f or entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and the second data [being] having been coded by a coding method; and

second program code means for arranging the first and the second data bits [such that] to store at least a bit of an N-order of the first data bits and at least a bit of [the N-order] an M-order of the second data bits [are stored] in one of the cells, the N and M being [an] different integral [number] numbers.

7. (Currently amended) The computer readable medium according to claim 6 further comprising:

third program code means for [generating at least a voltage] initiating generation of voltages corresponding to the [N-order] N- and M-order bits; and

fourth program code means for applying the voltage to the one of the cells in response to an address information corresponding to the one of the cells.

8. (Original) A semiconductor device comprising:

converting means for converting a logical address into a physical address;

a plurality of multilevel memory cells arranged so as to correspond to a physical address space including the physical address, each cell storing 2^n levels of data each expressed by n ($n \geq 2$) number of bits (Xl, X2, ..., Xn);

judging means for judging whether a logical address space including the logical address matches the physical address space;

specifying means for specifying the most significant bit Xl, by one-time specifying operation, by means of a reference value when the logical address space matches the physical address space; and

outputting means for outputting the specified bit from one of the cells corresponding to the physical address.

9. (Original) The semiconductor device according to claim 8 wherein each cell includes at least one transistor and the specifying means comprises:

first means for generating a voltage corresponding to the reference value;.

second means responsive to the physical address for generating an address signal;

third means responsive to the address signal for applying the voltage to one of the cells corresponding to the physical address;

fourth means f or determining whether a current flows between a source and a drain of

the transistor; and

fifth means for specifying the most significant bit Xl in accordance with a result of the determination.

10. (Original) The semiconductor device according to claim 8 wherein the specifying means comprises:

a comparator having a first input terminal connected to an output of each cell, a voltage corresponding to the most significant bit Xl being applied to the first input terminal; and

a voltage applying circuit, connected to a second input terminal of the comparator, for applying the voltage corresponding to the reference value to the second input terminal, the most significant bit Xl being specified in accordance with a result of comparison by the comparator.

11. (Original) The semiconductor device according to claim 8 wherein the specifying means specifies the bits (Xl, X2, . .., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

12. (Original) The semiconductor device according to claim 11 wherein each cell includes at least one transistor and the specifying means comprises:

first means for generating n number of voltages corresponding to the n number of reference values;

second means responsive to the physical address for generating an address signal;

third means responsive to the physical address for applying the voltages to one of the cells corresponding to the address signal;

fourth means for applying maximum the n number of voltages to a gate of the transistor at a specific voltage applying order until a current flows between a source and a drain of the transistor; and

means for specifying the bits (Xl, X2, ..., Xn) by detecting the current.

13. (Original) The semiconductor device according to claim 11 wherein the specifying means comprises:

a comparator having a first input terminal connected to an output of each cell, voltages corresponding to the bits (Xl, X2, ..., Xn) being applied to the first input terminal; and

a voltage applying circuit, connected to a second input terminal of the comparator, for applying voltages corresponding to maximum the n number of reference values to the second input terminal, the bits (Xl, X2, ..., Xn) being specified in accordance with a result of comparison by the comparator.

14. (Original) A method of reading n ($n \geq 2$) number of bits (Xl, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ..., Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit Xl, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

15. (Original) The method according to claim 14 further comprises the step of specifying the bits (Xl, X2, ..., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

16. (Original) A method of reading n ($n \geq 2$) number of bits (Xl, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ... and Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit Xl by applying a predetermined reference voltage to a gate of the transistor to determine whether a current flows between a source and a drain of the

transistor when the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

17. (Original) The method according to claim 16 further comprises the step of specifying the bits (Xl, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

18. (Original) A method of reading n ($n \geq 2$) number of bits (Xl, X2, ... Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ..., and Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit Xl by comparing an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

19. (Original) The method according to claim 18 further comprises the step of specifying the bits (X1, X2, ..., Xn) by comparing output voltages of the transistor corresponding to the bits (X1, X2, ..., Xn) with reference voltages corresponding to the bits (X2, ..., Xn).

20. (Original) A computer readable medium storing program code for causing a computer to read n ($n \geq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means fop judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

21. (Original) The computer readable medium according to claim 20 further comprising program code means for specifying the bits (X1, X2, ..., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

22. (Original) A computer readable medium storing program code for causing a computer to read n ($n \geq 2$) number of bits (Xl, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means for judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit Xl by applying a reference voltage to a gate of the transistor when the logical address space matches the physical address space to determine whether a current flows between a source and a drain of the transistor; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

23. (Original) The computer readable medium according to claim 22 further comprising the program code means for specifying the bits (Xl, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

24. (Original) A computer readable medium storing program code for causing a computer to read n ($n \geq 2$) number of bits (Xl, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means for judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit Xl by comparing an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

25. (Original) The computer readable medium according to claim 24 further comprising the program code means for specifying the bits (Xl, X2, ..., Xn) by comparing voltages corresponding to the bits (Xl, X2, ..., Xn) with reference voltages corresponding to the bits (Xl, X2, ..., Xn) when judged that the logical address space does not match the physical address space.

26. (Currently amended) A semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the semiconductor device comprising: [a bit disperser for dispersing bits over the plurality of multilevel memory cells to store the bits therein, the bits constituting at least one code data coded by a coding method to be

stored in the cells]

a controller for entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and second data having been coded by a coding method; and

a bit data separator for separating the first and second data bits to store at least a bit of an N-order of the first data bits and at least a bit of an M-order of the second data bits in one of the cells, the N and M being different integral numbers.

27. (Currently amended) The semiconductor device according to claim 26, wherein the bit [disperser] data separator controls the number of bits to be stored in at least one of the cells in accordance with capability of code error correction of the coding method.

28. (Currently amended) The semiconductor device according to claim 26, wherein the bit [disperser] data separator puts the bits of [M] O number of code data, each code data having a code length [N] P, into positions of arrangement in [M] O lines x [N] P rows and stores the [M] O number of bits in each cell, the [M] O and [N] P being an integral number.

29. (Original) The semiconductor device according to claim 26, wherein the multilevel memory cells are non-volatile semiconductor memories.

30. (Cancelled)

31. (Currently amended) A method of writing at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the method comprising the [step of dispersing bits constituting the code data over the plurality of multilevel memory cells] steps of:

entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and second data having been coded by a coding method; and

separating the first and second data bits to store at least a bit of an N-order of the first data bits and at least a bit of an M-order of the second data bits in one of the cells the N and M being different integral numbers.

32. (Cancelled)

33. (Original) A semiconductor device comprising:

inputting means for inputting a logical address;

converting means for converting the logical address into a physical address;

a plurality of multilevel memory cells arranged so as to correspond to physical addresses, each cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more;

controlling means for selecting one of the cells corresponding to the physical address and designating one of the data components in accordance with the logical address; and

outputting means for outputting the designated data component, wherein the semiconductor device has a judging value f or specifying, by one-time specifying operation, at

least one of the data components, and when the logical address is included in an address space Al that corresponds to an address space including the physical address, the controlling means specifies the designated data component by means of the judging value, thus the specified data being output by the outputting means.

34. (Original) The semiconductor device according to claim 33, wherein each cell stores 2^n levels of data each expressed by data components (Xl, X2, ..., Xn) of n - th dimension ($n \geq 2$), the semiconductor device having a first judging value for specifying, by one-time specifying operation, at least the data component Xl having data of the logical address included in the address space Al, when the logical address included in the address space Al is input by the inputting means, the data component Xl specified by the controlling means by means of the first judging value is output by the outputting means among the data components stored in the cell corresponding to the logical address included in the address space Al.

35. (Original) The semiconductor device according to claim 34, having judging values for specifying the data components (X2, Xn) of a logical address included in address spaces (A2, ..., An) close to the address space Al, wherein the data components (X2, ..., Xn) have the data stored sequentially in the order of closeness to the address space Al, the controlling means specifies a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including the logical address input by the inputting means, thus the data component Xk being output by the outputting means.

36. (Original) The semiconductor device according to claim 33, wherein each cell is provided with a control gate and a charge accumulating layer having a floating gate.

37. (Original) A method of reading data stored in a semiconductor device having at least one multilevel memory cell provided so as to correspond to a physical addresses converted from an input logical address, the cell having a control gate, a source and a drain, the cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more; comprising the steps of:

preparing a judging value for specifying at least one of the data components; and

applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an address space Al that corresponds to an address space including the physical address.

38. (Original) The method according to claim 37, wherein the cell stores 2^n levels of data each expressed by data components (Xl, X2, ..., Xn) of n - th dimension ($n \geq 2$), the data component Xl having data of the logical address included in the address space Al, further comprising the steps of:

preparing a first judging value for specifying at least the data component Xl;

specifying the data component Xl by means of the first judging value among data components corresponding to the input logical address included in the address space Al; and

outputting the data component Xl specified by means of the first judging value among data components corresponding to the input logical address included in the address space Al.

39. (Original) The method according to claim 38, further comprising the steps of:

preparing judging values for specifying the data components (X2, ..., Xn) having data of logical addresses included in address spaces (A2, ..., An) close to the address space Al, the data components (X2, ..., Xn) having the data stored sequentially in the order of closeness to the address space Al;

specifying a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including an input logical address; and

outputting the data component Xk.

40. (Original) A computer readable medium storing program code for causing a computer to read data stored in a semiconductor device having at least one multilevel memory cell provided so as to correspond to a physical addresses converted from an input logical address, the cell having a control gate, a source and a drain, the cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more; comprising:

first program code means for preparing a judging value for specifying at least one of the data components; and

second program code means f or applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an address space Al that corresponds to an address space including the physical address.

41. (Original) The computer readable medium according to claim 40, wherein the cell stores 2^n levels of data each expressed by data components (Xl, X2, ..., Xn) of n - th dimension ($n \geq 2$), the data component Xl having data of the logical address included in the address space Al, further comprising:

third program code means for preparing a first judging value for specifying at least the data component Xl;

fourth program code means for specifying the data component Xl by means of the first judging value among data components corresponding to the input logical address included in the address space Al; and

fifth program code means for outputting the data component Xl specified by means of the first judging value among data components corresponding to the input logical address included in the address space Al.

42. (Original) The computer readable medium according to claim 41, further comprising:

sixth program code means f or preparing judging values for specifying the data components (X2, ..., Xn) having data of logical addresses included in address spaces (A2, ..., An) close to the address space Al, the data components (X2, ..., Xn) having the data stored sequentially in the order of closeness to the address space Al;

seventh program code means for specifying a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including an input logical address; and

eighth program code means for outputting the data component Xk.

Application No.: 09/438,295 Docket No.: 21737-00013-US

Claims 43-68 cancelled.